Claims:

1. A ballast (10), comprising:

an inverter output stage (30); and

a power factor correction input stage (20) in electrical communication with said inverter output stage (30) to apply a regulated DC voltage as a function of a line voltage to said inverter output stage (30), said power factor correction input stage (20) including

a power factor correction integrated circuit (26), and

a line voltage sensing circuit (22) in electrical communication with said power factor correction integrated circuit (26) to apply a clamped rectified voltage to said power factor correction integrated circuit (26),

wherein said clamped rectified voltage is a function of a load being applied by said inverter output stage (30) to said power factor correction integrated circuit (26).

2. The ballast (10) of claim 1, wherein the clamped rectified voltage and the load being applied by said inverter output stage (30) to said power factor correction integrated circuit (26) are proportional.

3. The ballast (10) of claim 1, further comprising:

a dimming interface (40) in electrical communication with said power factor correction input stage (20) to communicate a dimming level signal as a function of an external ballast control signal to said power factor correction input stage (20),

wherein the dimming level signal is indicative of the load being applied by said inverter output stage (30) to said power factor correction integrated circuit (26).

4. The ballast (10) of claim 1,

wherein said inverter output stage (30) is in electrical communication with said power factor correction input stage (20) to communicate a load feedback signal to said power factor correction input stage (20); and

wherein the load feedback signal is indicative of the load being applied by said inverter output stage (30) to said power factor correction integrated circuit (26).

5. The ballast (10) of claim 1, wherein said line voltage sensing circuit (22) includes:

a voltage rectifier (23) operable to generate a rectified voltage as a function of the line voltage;

a THD controller (25) operable to generate a clamping voltage as a function of the load being applied by said inverter output stage (30) to said power factor correction integrated circuit (26); and

a voltage divider (24) in electrical communication with said voltage rectifier (23) and said THD controller (25) to generate the clamped rectified voltage as a function of the rectified voltage and the clamping voltage.

6. The ballast (10) of claim 5,

wherein said voltage divider (24) includes a dividing node (N1); and

wherein said THD controller (25) includes means for applying the clamping voltage to said dividing (N1) node of said voltage divider (24) as a function of the line voltage.

7. The ballast (10) of claim 6, wherein the clamping voltage and the line voltage are inversely proportional.

8. The ballast (10) of claim 5, further comprising:

a dimming interface (40) in electrical communication with said power factor correction input stage (20) to communicate a dimming level signal to said power factor correction input stage (20), the dimming level signal being indicative of the load being applied by said inverter output stage (30) to said power factor correction integrated circuit (26); and

wherein said THD controller (25) includes means for generating the clamping voltage as a function of the dimming level signal.

9. The ballast (10) of claim 5, further

wherein said inverter output stage (30) is in electrical communication with said power factor correction input stage (20) to communicate a load feedback signal to said power factor correction input stage (20);

wherein the load feedback signal being indicative of the load being applied by said inverter output stage (30) to said power factor correction integrated circuit (26); and

wherein said THD controller (25) includes means for generating the clamping voltage as a function of the load feedback signal.

10. The ballast (10) of claim 5,

where said power factor correction integrated circuit (26) including a multiplier input pin (MIP); and

wherein said voltage divider (25) includes a dividing node (N2) in electrical communication with said multiplier pin (MIP) to apply the clamped rectified voltage to said power factor correction integrated circuit (26).

11. A power factor correction input stage (20), comprising:

a power factor correction integrated circuit (26);

a line voltage sensing circuit (22) in electrical communication with said power factor correction integrated circuit (26) to apply a clamped rectified voltage as a function of a line voltage to said power factor correction integrated circuit (26),

wherein the clamped rectified voltage is a function of a load being applied by to said power factor correction integrated circuit (26).

12. The power factor correction input stage (20) of claim 11, wherein the clamped rectified voltage and the load being applied to said power factor correction integrated circuit (26) are proportional.

13. The power factor correction input stage (20) of claim 11, wherein said line voltage sensing circuit (22) includes:

a voltage rectifier (23) operable to generate a rectified voltage as a function of the line voltage;

a THD controller (25) operable to generate a clamping voltage as a function of the load being applied to said power factor correction integrated circuit (26); and

a voltage divider (24) in electrical communication with said voltage rectifier (23) and said THD controller (25) to generate the clamped rectified voltage as a function of the rectified voltage and the clamping voltage.

14. The power factor correction input stage (20) of claim 13,

wherein said voltage divider (24) includes a dividing node (N1); and

wherein said THD controller (25) includes means for applying the clamping voltage to said dividing (N1) node of said voltage divider (24) as a function of the line voltage.

15. The power factor correction input stage (20) of claim 11, wherein the clamping voltage and the line voltage are inversely proportional.

16. The power factor correction input stage (20) of claim 15,

where said power factor correction integrated circuit (26) including a multiplier input pin (MIP); and

wherein said voltage divider (25) includes a dividing node (N2) in electrical communication with said multiplier pin (MIP) to apply the clamped rectified voltage to said power factor correction integrated circuit (26).

17. A ballast (10), comprising:

an inverter output stage (30); and

a power factor correction input stage (20) in electrical communication with said inverter output stage (30) to apply a regulated DC voltage as a function of a line voltage to said inverter output stage (30), said power factor correction input stage (20) including

a power factor correction integrated circuit (26), and

means for applying a clamped rectified voltage to said power factor correction integrated circuit (26),

wherein said clamped rectified voltage is a function of a load being applied by said inverter output stage (30) to said power factor correction integrated circuit (26).

18. A power factor correction input stage (20), comprising:

a power factor correction integrated circuit (26);

means for applying a clamped rectified voltage as a function of a line voltage to said power factor correction integrated circuit (26),

wherein the clamped rectified voltage is a function of a load being applied by to said power factor correction integrated circuit (26).